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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,361	11/03/2003	Pierre Marty	S1022.80985US01	5357

7590 12/02/2005

EXAMINER	
GOGIA, ANKUR	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 12/02/2005

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,361	MARTY ET AL.	
	Examiner	Art Unit	
	Ankur Gogia	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/700,361 has a total of 18 claims pending in the application; there is 1 independent claim and 17 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Priority

3. Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 371 from PCT/FR01/02669 filed on 24 August 2001.

4. Acknowledgment is made of applicant's claim for foreign priority based on an application 00/10943 filed in France on 25 August 2000.

Drawings

5. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

6. As required by M.P.E.P. 609(c), the applicant's submission of the Information Disclosure Statement dated 3 November 2003 is acknowledged by the examiner and the cited references, with the exception of the International Search Report from PCT/FR01/002669, have been considered in the examination of the claims now pending. As required by M.P.E.P. 609(c)(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

7. The information disclosure statement filed 3 November 2003 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; **each non-patent literature publication or that portion which caused it to be listed**; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the International Search Report referred to therein has not been considered.

Specification

8. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Control circuit to enable high data rate access to a DRAM with a plurality of areas.

Claim Rejections - 35 USC § 103

9. Claims 1-3, 5-7 and 11-16 are rejected under 35 U.S.C. 103(a) as being obvious over Chan et al. (U.S. Pat. 5,822,772) in view of Munson et al. (U.S. PGPub 2001/0037444) and "Systems Architecture – Hardware and Software in Business Information Systems" by Stephen D. Burd.

Claim 1

Chan et al. disclose a circuit for controlling a memory including at least two areas to which access cannot be had simultaneously, the circuit including:

second means for detecting that a first instruction intended for a first area is a predetermined instruction to be followed by a period during which the first area can receive no other instruction **[On Pg. 6, Lines 3-5, Abstract Line 3 and in Fig. 3, Item18 of the instant specification the applicant discloses the second means as a circuit. In Col. 5, Line 60 Chan et al. disclose the selection logic as an element of a memory controller circuit and in Col. 5, Line 61 – Col. 6, Line 12 they disclose wherein the selection logic provides another command to the memory while a command from an active queue is currently running by using idle clock cycles of the active command. It is inherent to such logic that the logic be able to detect that the current active instruction has idle clock cycles. Since it is not a known constant whether a given instruction is going to have any idle clock cycles the logic must be told or must determine in some manner that the current active instruction has an idle clock cycle.]**, and

third means for, during said period, providing instructions to another memory area **[On Pg. 6, Lines 5-13, Abstract Line 4 and in Fig. 3, Item 20 of the instant specification the applicant discloses the third means as a circuit. In Col. 5, Line 60 Chan et al. disclose the selection logic as an element of a memory controller circuit and in Col. 5, Line 61 – Col. 6, Line 12 they disclose wherein the selection logic provides another command to another memory area while a command from an active queue is currently running on a first area, by using idle clock cycles of the active command.]**.

Chan et al. do not disclose expressly the first means **[In Fig. 4, Items 101-104 and Col. 5, Lines 50-59 Chan et al. disclose a set of queues that store memory access commands separately for each bank of memory cells in a DRAM, however in Pg. 5, Line 31 – Pg. 6, Line 1, Abstract Line 2 and Fig. 3, Items 14 and 16 of the instant specification the applicant discloses that the first means is a register set.]**.

It is well known in the art that a queue is synonymous with a group of registers as is shown by Munson et al. They disclose, in ¶45, a system for buffering instructions wherein the instructions are stored in **"a group of shift registers, or a first-in-first-out queue"**.

Chan et al. and Munson et al. are analogous art because they are from the similar problem solving area of buffering instructions in a processing environment.

Furthermore, the already modified invention of Chan et al. and Burd are analogous art because they are from the similar problem solving area of buffering instructions in a register.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Chan et al. and Munson et al. before them, to provide command registers for each bank of memory cells in a DRAM in an improved memory controller.

The motivation for doing so would have been that registers are the fastest form of temporary storage **(Burd: Pg. 204, Fig. 6-2)**.

Therefore, it would have been obvious to combine Munson et al. with Chan et al. for the benefit of storing instructions in a fast access memory as specified in claim 1.

Claim 2

Chan et al. further disclose wherein the each memory area is accessible via a specific cache. **[On page 1, lines 19-20 of the applicants admitted prior art, it states that a typical DRAM memory contains several memory areas each accessible via a cache. Chan et al. disclose a controller for a DRAM memory (Fig. 4, Item 100). Therefore, Chan et al. disclose wherein each memory area is accessible via a specific cache.]**

Claim 3

Chan et al. further disclose the circuit further including fourth means **(Fig. 3, Item 12; Spec. Pg. 5, Lines 30-32)** for receiving read and/or write requests and for writing each of them in the form of a series of instructions into the first means, each series of instructions including a predetermined number of data. **[Chan et al. disclose dispatch logic in fig. 4, item 121 and col. 5, lines 55-59 that receives memory access**

commands and dispatches the commands into a command queue according to which memory row (bank) in the DRAM that this command is accessing.]

Claim 5

Chan et al. further disclose wherein the predetermined number of data of a series of instructions includes an indication of whether the series of instructions aims at a reading from or at a writing into the memory **[(inherent); Since memory access commands are reads and writes the controller must know what type of request it receives or it will be unable to process the request since it will not be possible to determine if the controller is to place data into the memory or take data out. Therefore, the instructions must have an indication of whether they are a read or a write]**.

Claim 6

Chan et al. further disclose wherein the predetermined number of data of a series of instructions includes the addresses for which said series of instructions is intended **(Col. 5, Lines 63-67)**.

Claim 7

Chan et al. further disclose wherein the predetermined number of data of a series of instructions includes the instructions forming said series of instructions **[(inherent); All DRAM memory access commands consist of multiple instructions (i.e. a read is actually a precharge, active, and read, while a write is a precharge, active, and write). The system disclosed by Chan et al. consists of a DRAM memory (Fig. 4, Item 100) and therefore the series of instructions issued in the system must**

include the instructions that form the series of instructions. Furthermore, in Fig. 6 it is seen for example that Queue 1 contains command 1 and as shown in the steps, command 1 consists of the command 1 RAS1 and the command 1 CAS1.].

Claims 11, 13 and 15

The already modified invention of Chan et al. further discloses wherein the first means include, for each area of the memory, a predetermined number of registers. **[As discussed above with regards to claim 1, Fig. 4, Items 101-104 and Col. 5, Lines 50-59 of Chan et al. disclose a set of queues that store memory access commands separately for each bank of memory cells in a DRAM. Further, Munson et al. disclose in ¶45 that a queue is synonymous with a group of registers. Therefore, the already modified invention of Chan et al. discloses wherein the first means includes a predetermined number or registers.]**

Claims 12, 14 and 16

The already modified invention of Chan et al. further discloses wherein said predetermined number of registers includes index registers for managing the writing and the reading of the other registers of said predetermined number of registers, respectively by the fourth and second means **[(inherent); Chan et al. discloses a set of queues that store instructions in fig. 4, items 101-104 and as argued above with regards to claim 1 a queue is synonymous with a group of registers. Given that a set of registers or queues is being used to store a series of instructions, there must be additional registers that hold the addresses of the current head (reading index) and tail (writing index) of the queue or register set. The reason for this is**

that without this information the system would not know where to read and write data from the queue or register set.].

10. Claims 4, 9 and 10 are rejected under 35 U.S.C. 103(a) as being obvious over Chan et al. in view of Munson et al. and "Systems Architecture – Hardware and Software in Business Information Systems" by Stephen D. Burd as applied to claims 1 and 3 above and further in view of applicants admitted prior art (hereinafter referred to as AAPA).

Claim 4

The already modified invention of Chan et al. does not disclose expressly wherein the predetermined number of data of a series of instructions especially includes an indication of the priority order existing between each series of instructions stored in the first means

However, AAPA discloses the above limitation. **[(Pg. 1, Lines33-34); Note in the reference it states that when simultaneous requests are received, priority is given to the request from the device holding the highest priority. For it to be determined which device has the highest priority, the request must include an indication of the priority order between the simultaneous requests]**.

The already modified invention of Chan et al. and AAPA are analogous art because they are from the similar problem solving area of improving memory access speeds to a memory of DRAM type.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the already modified invention of Chan et al. and

AAPA before them, to include a priority parameter as part of the instruction in a memory access controller that processes requests simultaneously.

The motivation for doing so would have been to enable the proper handling of requests so that they are processed in order of highest importance to lowest importance **(AAPA, Pg. 1, Lines 33-34)**.

Therefore, it would have been obvious to combine AAPA with the already modified invention of Chan et al. for the benefit of ordered processing of requests to obtain the invention as specified in claim 4.

Claim 9

The already modified invention of Chan et al. further discloses wherein the first means include, for each area of the memory, a predetermined number of registers. **[As discussed above with regards to claim 1, Fig. 4, Items 101-104 and Col. 5, Lines 50-59 of Chan et al. disclose a set of queues that store memory access commands separately for each bank of memory cells in a DRAM. Further, Munson et al. disclose in ¶45 that a queue is synonymous with a group of registers. Therefore, the already modified invention of Chan et al. discloses wherein the first means includes a predetermined number or registers.]**

Claim 10

The already modified invention of Chan et al. further discloses wherein said predetermined number of registers includes index registers for managing the writing and the reading of the other registers of said predetermined number of registers, respectively by the fourth and second means **[(inherent); Chan et al. discloses a set**

of queues that store instructions in fig. 4, items 101-104 and as argued above with regards to claim 1 a queue is synonymous with a group of registers. Given that a set of registers or queues is being used to store a series of instructions, there must be additional registers that hold the addresses of the current head (reading index) and tail (writing index) of the queue or register set. The reason for this is that without this information the system would not know where to read and write data from the queue or register set.].

11. Claims 8, 17 and 18 are rejected under 35 U.S.C. 103(a) as being obvious over Chan et al. in view of Munson et al. and "Systems Architecture – Hardware and Software in Business Information Systems" by Stephen D. Burd as applied to claims 1 and 3 above and further in view of Kodama (U.S. Pat. 5,286,466).

Claim 8

The already modified invention of Chan et al. does not disclose expressly wherein the predetermined number of data of a series of instructions includes the duration necessary to execute said series of instructions.

Kodama discloses a parallel processing system where the instruction field of the each instruction includes an execution predict count information **(Abstract)**. This information provides the number of basic clock cycles required to execute the instruction **(duration necessary to execute the series of instructions)**.

The already modified invention of Chan et al. and Kodama are analogous art because they are from a similar problem solving area of efficiently processing instructions simultaneously.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of Kodama and the already modified invention of Chan et al. before them, to include in the instruction, an indication of the duration of that instruction.

The motivation for doing so would have been to equalize the period of time required to execute various instructions **(Kodama, Col. 1, Lines 54-57)**.

Therefore, it would have been obvious to combine Kodama with the already modified invention of Chan et al. for the benefit of equalizing the period of time required to execute various instructions to obtain the invention as specified in claim 8.

Claim 17

The already modified invention of Chan et al. further discloses wherein the first means include, for each area of the memory, a predetermined number of registers. **[As discussed above with regards to claim 1, Fig. 4, Items 101-104 and Col. 5, Lines 50-59 of Chan et al. disclose a set of queues that store memory access commands separately for each bank of memory cells in a DRAM. Further, Munson et al. disclose in ¶45 that a queue is synonymous with a group of registers. Therefore, the already modified invention of Chan et al. discloses wherein the first means includes a predetermined number or registers.]**

Claim 18

The already modified invention of Chan et al. further discloses wherein said predetermined number of registers includes index registers for managing the writing and the reading of the other registers of said predetermined number of registers,

respectively by the fourth and second means **[(inherent); Chan et al. discloses a set of queues that store instructions in fig. 4, items 101-104 and as argued above with regards to claim 1 a queue is synonymous with a group of registers. Given that a set of registers or queues is being used to store a series of instructions, there must be additional registers that hold the addresses of the current head (reading index) and tail (writing index) of the queue or register set. The reason for this is that without this information the system would not know where to read and write data from the queue or register set.]**.

Relevant Art Cited by the Examiner

12. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See M.P.E.P. 707.05(c).

The following references teach improved memory controllers that provide high data rate access to the memory.

U.S. Patent/Pub. Number	Relevant Sections
6,392,935	Fig. 3c
6,212,611	Fig. 1
6,389,520	Figs. 5 and 6
5,903,509	Figs. 7 and 8

Conclusion

13. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

Per the instant office action, claims 1-18 have received a first action on the merits and are subject of a first action non-final.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ankur Gogia whose telephone number is 571-272-4166. The examiner can normally be reached on M-F 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A. M.

Ankur Gogia
Examiner
Art Unit 2187

11/23/05

Donald Sparks

DONALD SPARKS
SUPERVISORY PATENT EXAMINER